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EXAMINER	
PERVAN, MICHAEL	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,847	KIMURA, HAJIME	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/15/04 9/1/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 8, 11, 13-14, 17-21 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Noboru et al (JP 2001-296873; as submitted by applicant).

In regards to claim 1, Noboru discloses a current drive circuit which supplies a signal current to a node of a driven circuit through a signal line,

wherein a precharge means for supplying a precharge voltage to the node through the signal line is provided (paragraphs 14-15); and

the precharge means has a supply means for supplying the precharge voltage to the node and the signal line prior to supplying the signal current (paragraphs 14-15).

In regards to claim 2, Noboru discloses the current drive circuit according to claim 1,

wherein the precharge means comprises a setting means for setting the precharge voltage to a potential equal to or according to a potential of the node in a stationary state when the signal current is supplied to the driven circuit (paragraphs 14-15).

In regards to claim 3, Noboru discloses the current drive circuit according to claim 1,

wherein the precharge means comprises a plural setting means for setting a plurality of the precharge voltages (paragraphs 14-15 and 18); and

a selection supply means for selectively supplying the precharge voltage to the node and the signal line according to a magnitude of the signal current (paragraphs 14-15 and 18).

In regards to claim 4, Noboru discloses a current drive circuit which supplies a signal current to a node of a driven circuit through a signal line, comprising:

a precharge circuit for supplying a precharge voltage to the node and the signal line (paragraphs 14-15 and 18);

a generation means for supplying the signal current to the precharge circuit and generating the precharge voltage (paragraphs 14-15 and 18); and

a supply means for supplying the precharge voltage to the node and the signal line prior to supplying the signal current to the driven circuit (paragraphs 14-15 and 18).

In regards to claim 5, Noboru discloses a current drive circuit which supplies a signal current to a node of a driven circuit through a signal line, comprising:

a precharge circuit for supplying a precharge voltage to the node (paragraphs 14-15); and

a supply means for generating the precharge voltage in advance by supplying a current corresponding to the signal current to the precharge circuit and then supplying the precharge voltage to the node and the signal line prior to supplying the signal current to the driven circuit (paragraphs 14-15).

In regards to claims 8 and 31, Noboru discloses the current drive circuit according to claim 4, comprising:

a plural setting means for setting a plurality of the precharge voltages (paragraphs 14-15 and 18); and

a selection supply means for selectively supplying the precharge voltage to the node and the signal line according to a magnitude of the signal current (paragraphs 14-15 and 18).

In regards to claim 11, Noboru discloses a display device comprising:

an image circuit to which an image data is provided as a current through a current line (paragraphs 14-18); and

a current drive circuit for supplying the image data to the current line as a signal current, wherein the current drive circuit comprising (paragraphs 14-18):

a source driver current source for supplying a signal current according to the image data from a node to the current line (paragraphs 14-18);

a precharge circuit for supplying a precharge voltage to the node and the current line (paragraphs 14-18); and

a supply means for supplying the precharge voltage to the node and the current line prior to supplying the signal current (paragraphs 14-18).

In regards to claim 13, Noboru discloses a display device comprising: a pixel circuit comprising a signal line for transmitting image data as a signal current (paragraphs 14-18) and a first driving element for supplying a driving current in proportion to the signal current from a power supply line (paragraphs 14-18); and

a source driver circuit comprising an image signal input current source for supplying the signal current to the signal line (paragraphs 14-18), wherein a precharge circuit for precharging the signal line prior to supplying the signal current to the signal line is integrated in the source driver circuit (paragraphs 14-18).

In regards to claim 14, Noboru discloses the display device according to claim 13, wherein the precharge circuit is selectively connected between the image signal input current source and the power supply line and comprises a second driving element for outputting a precharge voltage according to the signal current (paragraphs 14-18).

In regards to claim 17,noboru discloses the display device according to claim 13, comprising:

a means for setting the precharge voltage to a value equal to or according to a voltage in a stationary state when the signal current is supplied to the first or the second driving element (paragraph 18).

In regards to claim 18, Noboru discloses a current drive circuit comprising:

a driven circuit (paragraphs 14-18);

a precharge circuit (paragraphs 14-18);

a means for controlling a connection between a driven circuit and a precharge circuit (paragraphs 14-18); and

a means for controlling a connection between a driven circuit and a current source circuit (paragraphs 14-18).

In regards to claim 19, Noboru discloses a current drive circuit comprising:

a driven circuit (paragraphs 14-18);

a precharge circuit (paragraphs 14-18);

a current source circuit for inputting a signal current to the driven circuit (paragraphs 14-18);

a means for controlling a connection between the driven circuit and the precharge circuit (paragraphs 14-18);

a means for controlling a connection between the driven circuit and the current source circuit (paragraphs 14-18); and

a means for outputting a voltage by amplifying a signal outputted from the precharge circuit (paragraphs 14-18).

In regards to claim 20, Noboru discloses a current drive circuit comprising:

a driven circuit (paragraphs 14-18);

a precharge circuit (paragraphs 14-18);

a current source circuit for inputting a signal current to the driven circuit (paragraphs 14-18);

a means for controlling a connection between the driven circuit and the precharge circuit (paragraphs 14-18);

a means for controlling a connection between the driven circuit and the current source circuit, wherein the precharge circuit outputs a precharge voltage selected from a plurality of voltage values (paragraphs 14-18).

In regards to claim 21, Noboru discloses a current drive circuit comprising:

a driven circuit (paragraphs 14-18);

a precharge circuit (paragraphs 14-18);

a current source circuit for inputting a signal current to the driven circuit (paragraphs 14-18);

a means for controlling a connection between the driven circuit and the precharge circuit (paragraphs 14-18);

a means for controlling a connection between the driven circuit and the current source circuit (paragraphs 14-18); and

a means for amplifying a signal outputted from the precharge circuit (paragraphs 14-18), wherein the precharge circuit outputs a precharge voltage selected from a plurality of voltage values (paragraphs 14-18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-7, 9-10, 12, 15-16, 22-30 and 32-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noboru et al.

In regards to claims 6 and 29, Noboru discloses the current drive circuit according to claims claim 4,

wherein the driven circuit comprises a first driving element and the precharge circuit comprises a second driving element (paragraph 15; first driving element (driving source 15) and second driving element (driving source 17)).

Noboru does not disclose the first and the second driving elements are the same in size or in size according to it.

However, Noboru discloses first and second driving elements having sizes (Fig. 1).

Since, there is no benefit or advantage in the specification for having the first and second driving elements being the same size, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either the first and second driving element with the same size or the first and second driving element with the same size based on a designer's choice.

In regards to claims 7, 12, 15, 30 and 36-37, Noboru does not disclose the current drive circuit according to claim 4, comprising:

a means for supplying the precharge voltage to the node and the signal line through an impedance transformation amplifier.

However, Noboru discloses supplying a precharge voltage by pulse amplitude modulation (paragraph 18).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Noboru to supply the precharge voltage to the node and the signal line via an impedance transformation amplifier since impedance conversion for applying voltage is well known.

In regards to claims 9, 24, 32-33 and 44-46, Noboru does not disclose the current drive circuit according to claim 1, comprising:

a means for setting a precharge period T_b for supplying the precharge voltage to the node and the signal line so as to satisfy $T_b = R_L \times C_L$ based on a wiring resistance R_L and a parasitic capacitance C_L of the signal line.

However, Noboru discloses the time amount is changed to be proportional according to the magnitude of the signal current (paragraph 18).

Since, there is no benefit or advantage given in the specification as to choosing a precharge period T_b so as to satisfy $T_b = R_L \times C_L$, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either time amount is changed to be proportional according to the magnitude of the signal current or a precharge period T_b so as to satisfy $T_b = R_L \times C_L$ based on a designer's choice.

In regards to claims 10 and 34-35, Noboru does not disclose the current drive circuit according to claim 9, comprising:

a means for setting as $T_a = T_b$ in the case where a supply period T_a of the signal current to the driven circuit satisfies $T_a < T_b$.

However, Noboru discloses the time amount is changed to be proportional according to the magnitude of the signal current (paragraph 18).

Since, there is no benefit or advantage given in the specification as to choosing a precharge period $T_a = T_b$ so as to satisfy $T_a < T_b$, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either time amount is changed to be proportional according to the magnitude of the signal current or a precharge period $T_a = T_b$ so as to satisfy $T_a < T_b$ based on a designer's choice.

In regards to claim 16, Noboru discloses a display device comprising:

a pixel circuit comprising (paragraphs 14-18; EL matrix) a signal line (11) for transmitting image data as a signal current and a first driving element for supplying a driving current in proportion to the signal current from a power supply line (paragraphs 14-18); and

a source driver circuit comprising an image signal input current source for supplying the signal current to the signal line (paragraphs 14-18), wherein a precharge circuit for precharging the signal line prior to supplying the signal current to the signal line is integrated in the source driver circuit (paragraphs 14-18);

the precharge circuit is selectively connected between the image signal input current source and the power supply line and comprises a second driving element for outputting a precharge voltage according to the signal current (paragraphs 14-18; precharge circuit is selectively connected by signal-line switch (DSW)).

Noboru does not disclose the first and the second driving elements are the same in size or in size according to it.

However, Noboru discloses first and second driving elements having sizes (Fig. 1).

Since, there is no benefit or advantage in the specification for having the first and second driving elements being the same size, it would have been obvious to one of ordinary skill in the art at the time of invention to choose either the first and second driving element with the same size or the first and second driving element with the same size based on a designer's choice.

In regards to claim 22, Noboru does not disclose the current drive circuit according to claim 18, wherein the driven circuit comprises a first transistor and the precharge circuit comprises a second transistor.

However, Noboru discloses having driven circuit (driving source 15) and precharge circuit (driving source 17) (paragraph 15).

Since, there is no benefit or advantage given in the specification for choosing to have a first and second transistor instead of first and second driving sources, it would have been obvious to one of ordinary skill in the art to choose either having first and second transistor or first and second driving sources based on a designer's choice.

In regards to claim 23, Noboru does not disclose the current drive circuit according to claim 22, wherein a proportion of a channel width W and a channel length L of the first transistor and a proportion of a channel width W and a channel length L of the second transistor are almost equal to each other.

However, Noboru discloses driving sources (15, 17), which has size and dimensions (Fig. 1).

Since, there is no benefit or advantage given in the specification for having the proportion of width and length of the first transistor to the second transistor being equal instead of not being equal, it would have been obvious to one of ordinary skill in the art to choose either having the proportion of width and length of the first transistor to the second transistor being equal or the proportion of width and length of the first transistor to the second transistor not being equal based on a designer's choice.

In regards to claim 25, Noboru does not disclose the current drive circuit according to claim 18, comprising:

a means for driving the driven circuit with a binary signal voltage.

However, Noboru discloses using pulse amplitude modulation (paragraph 18).

Since, there is no benefit or advantage given in the specification for choosing a binary signal voltage instead of Pulse Amplitude Modulation, it would have been obvious to one of ordinary skill in the art to choose either a binary signal voltage or Pulse Amplitude Modulation based on a designer's choice.

In regards to claims 26 and 50-52, Noboru discloses the current drive circuit according to claim 18,

the precharge circuit and the current source circuit are disposed in a source driver circuit of the display device (paragraph 14-18).

Noboru does not disclose wherein the driven circuit is disposed in a pixel of a display device.

However, Noboru discloses the driven circuit is disposed in a reference current source circuit (paragraph 14-18).

Since, there is no benefit or advantage given in the specification for choosing to have the driven circuit disposed in a pixel instead of a reference current source circuit, it would have been obvious to one of ordinary skill in the art to choose either having driven circuit disposed in a pixel or a reference current source circuit based on a designer's choice.

In regards to claims 27 and 53-55, Noboru discloses the current drive circuit according to claim 18,

the precharge circuit and the current source circuit are disposed in a reference current source circuit (paragraph 14-18).

Noboru does not disclose wherein the driven circuit is disposed in a digital voltage/analog current conversion circuit.

However, Noboru discloses the driven circuit is disposed in a reference current source circuit (paragraph 14-18).

Since, there is no benefit or advantage given in the specification for choosing to have the driven circuit disposed in a pixel instead of a reference current source circuit, it would have been obvious to one of ordinary skill in the art to choose either having driven circuit disposed in a pixel or a reference current source circuit based on a designer's choice.

In regards to claims 28 and 56-58, Noboru does disclose the current drive circuit according to claim 18,

wherein the precharge circuit comprises a transistor; and

a gate and a drain of the transistor are connected to each other.

However, Noboru discloses the precharge circuit comprising a switch (Fig. 1).

Since, there is no benefit or advantage in the specification for choosing a transistor instead of a switch, it would have been obvious to one of ordinary skill in the art at the time of invention to choose a precharge circuit comprising either a transistor or a switch based on a designer's choice.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP
Mar. 1, 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER